Po Jui (Elton) Shih

CONTACT INFORMATION

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EDUCATION

Cornell University — **Ithaca, NY, USA**
Ph.D. in Electrical and Computer Engineering — 2024 - 2030 (*Expected*)

- Research focus: *Hardware-Software Co-Design*, *Computer Architecture*, *Computer Systems*
- Advisor: *Prof. Christopher Batten*

University of New South Wales (UNSW) — **Sydney, Australia**
B.Eng. (Class I Honours) in Computer Engineering, WAM: 84/100 — 2018 - 2021

- Thesis title: *Hardware Accelerated Real-Time Selective Genome Sequencing*
- Advisors: *Prof. Sri Parameswaran, Dr. Hasindu Gamaarachchi*

WORK AND RESEARCH EXPERIENCE

Computer Systems Lab, Cornell University — **Ithaca, NY, USA**
PhD Student — Aug 2024 - *Present*

- Researching hardware–software co-design toward unifying specialization and programmability. The goal is to discover principles that allow high-level programs to be mapped efficiently across heterogeneous systems without explicit hardware-specific coding.
- Designed SMX [MICRO'25], which introduces an 1D vector ISA extension and a 2D tiled tightly coupled co-proessor for efficient universal sequence alignment.
- Built a gem5–Verilator co-simulation framework for full-system RTL accelerator evaluation as part of the Cornell ECE6745 project.
- Exploring efficient mapping of dynamic programming workloads on the rack-scale Hammerblade manycore

CTO Office, Audinate — **Sydney, Australia**
Research Engineer II — Aug 2022 - Jul 2024
Research Engineer I — Jan 2022 - Aug 2023
Research and Development Engineering Intern — Winter 2021
Research and Development Engineering Intern — Summer 2020
Research and Development Engineering Intern — Summer 2019

- Led embedded systems and networking R&D within the CTO Office, driving cross-team and cross-company projects from prototype to production.
- Developed high-performance packet I/O for Dante audio over IP using XDP and AF_XDP, implementing a low-latency fast path with queue steering.
- Ported Dante across embedded Linux, Android, and Zephyr RTOS on custom boards, RISC-V, DSPs, and asymmetric MCU systems; owned bring-up, drivers, and containerized deployment.
- Researched real-time networking across RTOS and embedded Linux, including jitter analysis, memory protection, and hard real-time scheduling with Xenomai; extended protocols with QUIC and evaluated efficient encryption for RTOS audio.
- Improved build and deployment infrastructure (cross-platform CI/CD, container runtime security, ccache) and mentored interns.

School of CSE, UNSW — **Sydney, Australia**
Casual Academic — Feb 2020 - Dec 2023

- Mentored students, taught tutorials and labs, delivered guest lectures, and co-designed a new hardware–software co-design course.

Embedded Systems Research Group, UNSW **Sydney, Australia**

Undergraduate Researcher Nov 2020 - May 2022

- Developed a hardware–software co-design for real-time nanopore adaptive sampling on the edge, leading to an Outstanding Thesis Award and a GigaScience publication.

PUBLICATIONS

1. Max Doblas, **Po Jui Shih**, Oscar Lostes-Cazorla, Miquel Moretó, Christopher Batten, and Santiago Marco-Sola. SMX: Heterogeneous Architecture for Universal Sequence Alignment Acceleration. *MICRO-58*, 2025.
2. **Po Jui Shih**, Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachchi. Efficient real-time selective genome sequencing on resource-constrained devices. *GigaScience 12 (giad046)*, 2023.

TALKS

1. Towards an Edge Algorithm-Hardware Co-Design Framework for Adaptive Sampling. *Workshop on Architecture for Health (Arch4Health), held in conjunction with MICRO-58*, Oct 2025.
2. Transitioning from FreeRTOS to Zephyr RTOS: A Product Refresh Journey. *Everything Open 2024*, Apr 2024.
3. Efficient real-time selective genome sequencing on resource-constrained devices. *ABACBS & COMBINE Symposium 2023*, Dec 2023.
4. Hardware accelerated real-time selective genome sequencing. *Outstanding Undergraduate Thesis Showcase, UNSW School of CSE*, Dec 2021.

TEACHING EXPERIENCE

Spring 2026, ECE6745 Complex Digital ASIC Design, *Head TA*, Cornell University
2023 Term 3, COMP3601 Design Project A (HW-SW Co-Design), *Guest lecturer*, UNSW
2023 Term 2, DESN2000 Eng Design & Prof Practice (COMP), *TA & Guest lecturer*, UNSW
2022 Term 3, COMP3601 Design Project A (HW-SW Co-Design), *Course designer & lecturer*, UNSW
2021 Term 3, COMP3601 Design Project A (HW-SW Co-Design), *TA*, UNSW
2021 Term 2, COMP1521 Computer Systems Fundamentals, *TA & Lab Assistant*, UNSW
2020 Term 1, COMP2121 Microprocessors and Interfacing, *TA*, UNSW

HONORS AND AWARDS

MICRO Travel Grant (2025)
Cornell Graduate Fellowship (2024), Cornell University
First Class Honours (2021), UNSW Faculty of Engineering
Outstanding Undergraduate Thesis (2021), UNSW School of CSE
Dean's Honours List (2018 - 2020), UNSW Faculty of Engineering

PROFESSIONAL SERVICES

External Reviewer: *ASP-DAC 2024*

PROFESSIONAL MEMBERSHIPS

ACM Student Member

SKILLS

Programming: *C/C++*, *Python*, *Go*, *System Verilog*,*VHDL*
Hardware/Simulation: *Verilator*, *gem5*, *Vivado*, *Vitis HLS*, *Quartus*
Systems/Networking: *XDP*, *eBPF*, *Wireshark*, *JTAG/OpenOCD*, *container runtimes*
RTOS: *Zephyr*, *FreeRTOS*, *ThreadX*
Build/OS: *Buildroot*, *Yocto*, *AOSP*

OTHER/PERSONAL

Languages: *English* (native proficiency), *Traditional Chinese Mandarin* (native proficiency)
Citizenship: *Australian*